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A THREE-LEVEL BOOST T-TYPE INVERTER UNDER NORMAL AND FAILURE OF SEMICONDUCTOR DEVICE MODES

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SUMMARY OF PH.D. THESIS

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PUBLICATIONS

Order	Paper	Publication Title	Year
01	A New Topology of Single-Phase Common Ground Buck-Boost Inverter with Component Voltage Rating Reduction	IEEE Access	2023
02	A Novel Three-Level Quasi-Switched Boost F-Type Inverter With High Voltage Gain and Self-Balanced Neutral-Point Voltage	IEEE Access	2023
03	Fault Tolerant Control Methods for Three-Level Boost T-Type Inverter	IEEE Transactions on Industrial Electronics	2022
04	Space Vector Modulation Method-Based Common Mode Voltage Reduction for Active Impedance-Source T-Type Inverter	IEEE Access	2022
05	An DPWM for Active DC-Link Type Quasi-Z-Source Inverter to Reduce Component Voltage Rating	Energies	2022
06	An SVM Scheme for Three-Level Quasi-Switched Boost T-Type Inverter With Enhanced Voltage Gain and	IEEE Transactions on Power Electronics	2021

	Capacitor Voltage Balance		
07	Enhanced Boost Factor for Three-Level Quasi-Switched Boost T-Type Inverter	Energies	2021

CONTENTS

Chapter 1:

OVERVIEW

1.1. Overview of the voltage gain enhancement scheme and neutral voltage balancing

In single-stage inverter circuits, two main issues that need special attention are: voltage gain and voltage balance across capacitors because they directly affect the voltage applied across the components, conversion efficiency, and output voltage quality. There are a lot of publications regarding boost factor improvements for single-stage inverter configurations. The highest boost factor achieved is $2/(1 - 2D)$, with D being the short-through (ST) factor of the inverter side. However, the ST duty ratio D is limited by $(1 – M)$, where M is modulation index of the inverter. This reduces the voltage gain of the inverter.

For the problem of capacitor voltage balancing, two main methods have been applied: 1) use an appropriate pulse width modulation (PWM) method or use closed loop controllers, 2) use a configuration capable of self-balancing the voltage across the capacitors. Publications using the first method for single-stage inverters typically adjust the upper ST (UST) and lower ST (LST) duty ratios to balance neutral-point voltage. In addition, small vectors of P-type, N-type are also considered in addition to the main switching sequence of the inverter to obtain neutral voltage balancing. In general, this method requires complicated calculations. For the second method, the switched-capacitor structure is the most commonly used configuration. By paralleling two capacitors in the ST state, the different between them can self-balanced without the use of sensors. However, there is still a certain difference between the voltage values on the capacitors caused by the parasitic elements on the components. Usually, the differential voltage accounts for about 4% of the average value of the capacitor voltages. In addition, due to the low parasitic resistance of the components, connecting two capacitors in parallel often creates a high value of current stress through the semiconductor devices.

In general, the above schemes and configurations have some main disadvantages, as follows: 1) having low voltage gain; 2) the method of balancing capacitors has many limitations, such as complicated calculations, affecting the gain of the system. Therefore, this thesis presents a space vector modulation (SVM) method to overcome these disadvantages. The 3-phase 3-level quasi-switched boost T-type inverter configuration (3L-qSBT^{2}I) was selected as the object to apply the proposed scheme. In this scheme, small vectors are used to obtain the neutral voltage balancing and insert UST and LST states to enhance the voltage gain of the inverter. Expected results can be stated as: 1) improved inverter gain; 2) improving component voltage rating; and 3) a simple and effective balancing scheme that does not affect the buck-boost operation of the inverter circuit.

1.2. Overview of the common-mode voltage reduction method for single-stage inverter configuration

Common-mode voltage (CMV) is one of the important problems in voltage-source inverters. CMV is the main cause of leakage current, shaft voltage, motor bearing current, and electromagnetic interference. In addition, high leakage currents lead to system instability.

In order to inherit the advantages of high voltage gain introduced in the previous study, this thesis further presents an SVM control method to reduce CMV. All vectors that produce high CMV values will be removed from the space vector diagram. Vectors with low CMV amplitudes are used to synthesize reference vectors. In this method, small vectors are still used to insert UST and LST states to enhance the voltage gain of the inverter.

1.3. Overview of the fault-tolerant method for open-circuit fault of semiconductor devices.

In recent years, inverter circuits based on semiconductor devices operating at high frequency have attracted many researchers around the world because of their advantages, such as: high power density, good output voltage quality, high

efficiency, … However, these semiconductors can face with failures that reduces system reliability. In some applications that require continuous of power supply, such as public transport systems and medical systems, these failures can lead to serious damage. Therefore, inverters need to be designed to operate in failure modes of semiconductor devices to improve system stability.

From the above analysis, this thesis further presents some PWM methods to solve the open-circuit fault (OCF)/ short-circuit fault (SCF) problems of the three-level boost T-type inverter (TLB-T^{2}I) in order to overcome the existing disadvantages of the traditional methods. The advantages of the proposed method can be listed as follows: 1) reducing the component voltage rating; 2) solving one or more OCFs of the transistors; 3) overcome the SCF of the semiconductor components on impedance-source circuit; and 4) overcome the OCF at the capacitors.

Chapter 2:

PROPOSED SVM SCHEME FOR 3L-qSBT^{2}I CONFIGURATION

2.1. 3L-qSBT^{2}I configuration.

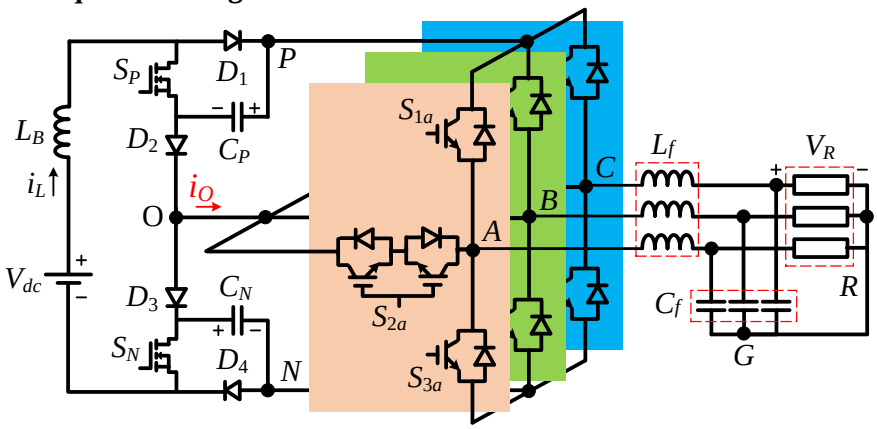

Figure 2.1. 3L-qSBT^{2}I configuration.

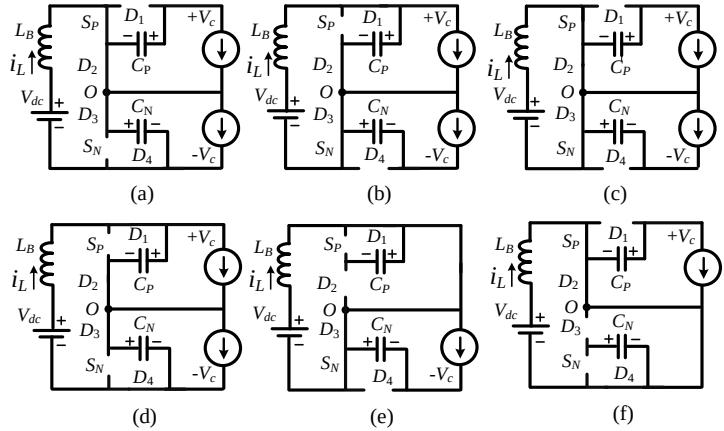

Figure 2.2. The operating modes of 3L-qSBT^{2}I (a) NST 1, (b) NST 2, (c) NST 3, (d) NST 4, (e) UST, (f) LST.

Similar to other single-stage inverter configurations, the 3L-qSBT^{2}I configuration operates in two main modes, ST mode and non-ST (NST) mode, as shown in Figure 2.2. However, in ST mode, two states of the UST and the LST will be used instead of the full-ST (FST) state to enhance the DC-link voltage, as shown in Figs. 2.2(e), 2.2(f). These two states will be inserted into small vectors of the N-type and P-type small vectors in order not to affect the output voltage of the inverter.

2.2. The proposed space vector modulation scheme

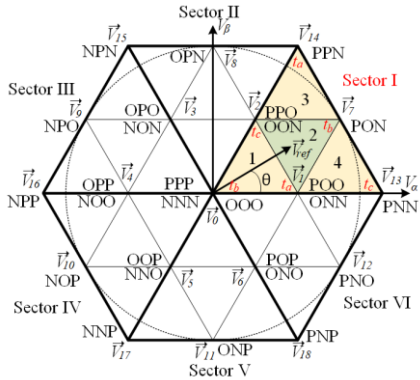

Figure 2.3. Space vector diagram for the proposed scheme.

2.2.1. Dwell-time calculation

Table 2.1. Dwell-times calculation for candidate vectors of sector I.

Region	t_a	t_b	t_c
1	$2MT_s\sin(\pi/3-\Theta)$	$T_s-2MT_s\sin(\pi/3+\Theta)$	$2MT_s\sin(\Theta)$
2	$T_s-2MT_s\sin(\Theta)$	$2MT_s\sin(\pi/3+\Theta)-T_s$	$T_s-2MT_s\sin(\pi/3-\Theta)$
3	$2MT_s\sin(\Theta)-T_s$	$2MT_s\sin(\pi/3-\Theta)$	$2T_s-2MT_s\sin(\pi/3+\Theta)$
4	$2T_s-2MT_s\sin(\pi/3+\Theta)$	$2MT_s\sin(\Theta)$	$2MT_s\sin(\pi/3-\Theta)-T_s$

Table 2.1. presents on-times 4 regions in sector I. Other sectors can also apply the same method to calculate the on-times.

2.2.2. Selection of switching sequence to balance neutral voltage

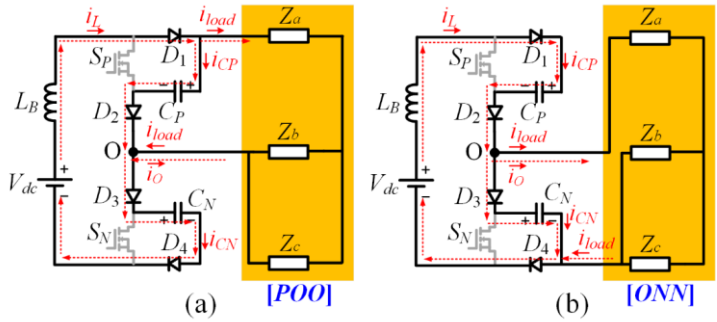

Figure 2.4. Effect of small vectors of form P and N on voltage across capacitors (a) small vector of form P [POO], (b) small vector of form N [ONN].

As shown in Figure 2.4, each small vector has two forms, the P-form small-vector and the N-form small vector. These two forms produce the same output line voltage value. Therefore, substituting these forms for each other does not affect the output voltage. However, each form has different effects on the neutral voltage. Specifically described as follows:

For the vector [POO], figure 2.4(a), it can be seen that the current flowing through the capacitor C_P has a smaller value than the current flowing through the capacitor C_N. Therefore, the voltage across the C_P capacitor will tend to

increase more slowly than the voltage across the C_N capacitor, assuming that the two capacitors have the same capacitance. Similarly, when vector [ONN] is used as shown in Figure 2.4(b), the voltage across the C_P capacitor tends to rise faster than the voltage across the capacitor C_N.

Based on the above analysis, the neutral voltage balancing can be divided into two cases as follows: 1) capacitor C_P voltage is greater than capacitor C_N voltage, 2) capacitor C_N voltage is greater than capacitor C_P voltage.

In case 1, $V_{CP}>V_{CN}$, P-type small vectors are used instead of N-type small vectors to enhance the voltage of the C_N capacitor and reduce the voltage of the capacitor C_P. At this time, the switching sequence for region 2 of sector I is defined as follows: [POP] - [POO] - [POO] - [POO] - [POO], and return.

For case 2, $V_{CP} < V_{CN}$, the proposed method uses N-type small vector instead of a P-type small vector to enhance the voltage of the capacitor C_P and reduce the voltage of the capacitor C_N. At this time, the switching sequence is defined as follows: [ONN] - [PON] - [OON] - [ONN] and return.

In order to ensure the buck/boost characteristic of the inverter, the UST and LST states are inserted into the switching sequence mentioned above, as shown in Figure 2.5.

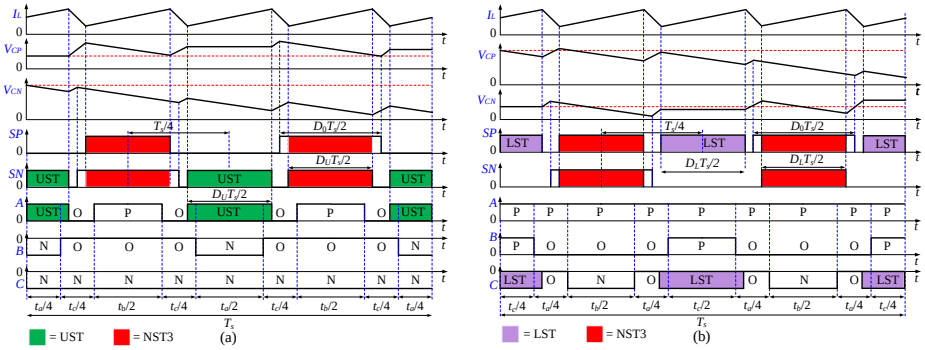

Figure 2.5. Proposed switching sequence for region 2 of sector I, UST and LST insertions and control signals of switches S_P, S_N.

2.2.3. Analysis of the steady state

The peak value of the output phase voltage is determined as follows:

$$V_{x,peak} = \frac{2}{\sqrt{3}} M V_C = \frac{2}{\sqrt{3}} \cdot \frac{M \cdot V_{dc}}{2 - 3D_{ST} - D_0} \tag{2.1}$$

The relationship between D_{ST} and M is determined as follows:

$$D_{ST} = 2 \times (1 - M) \tag{2.2}$$

The relationship between D_0 and D_{ST} is shown as follows:

$$D_{ST} \le D_0 \le 1 - D_{ST} \tag{2.3}$$

2.3. Comparison study.

The proposed scheme improves the voltage gain and reduces component voltage ratings.

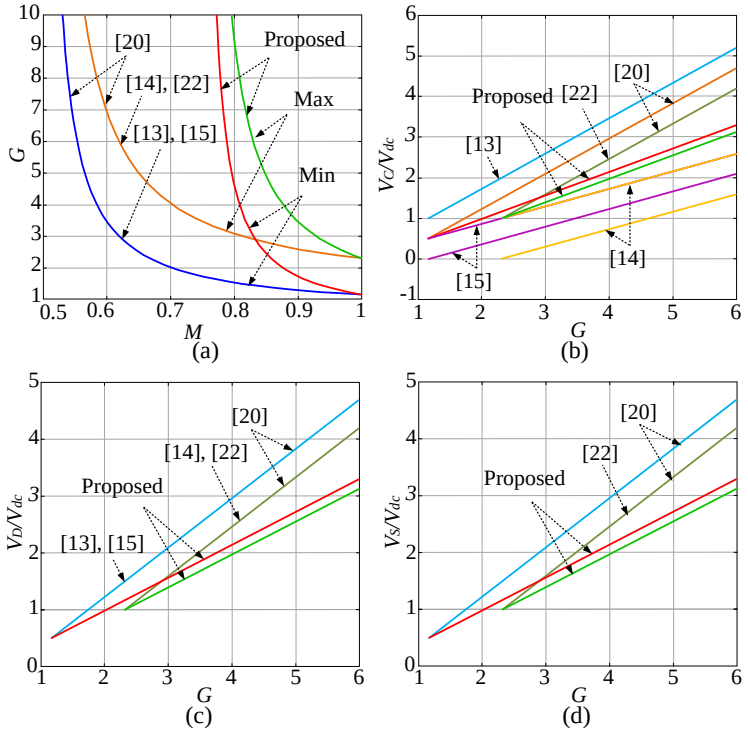

Figure 2.7. (a) M and G, (b) G and capacitor voltage rating, (c) G and diode voltage rating, (d) G and voltage stress of S_P/S_N.

2.4. Experiment with the proposed SVM scheme

Table 2.2 Experimental parameters

Components/Parameters		Values
Input DC voltage	V_{dc}	70 V – 210 V
Output RMS voltage	$V_{x,RMS}$	110
Inverter frequency	f_0	50 Hz
Switching frequency	f_s	10 kHz
Input inductor	L_B	3 mH/20 A
Capacitor	C_P and C_N	1 mF/400 V
LC filter	L_f and C_f	3 mH and 10 µF
R load	R	56Ω

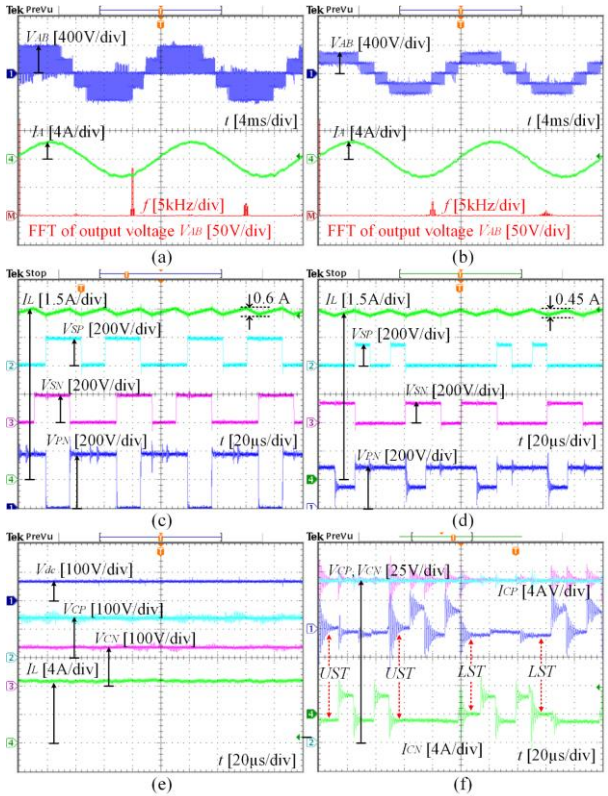

Figure 2.8. Experimental results of 3L-qSBT^{2}I with the proposed scheme and [20] when V_{dc} = 70 V: (a), (c) method [20], (b), (d), (e), (f) proposed method.

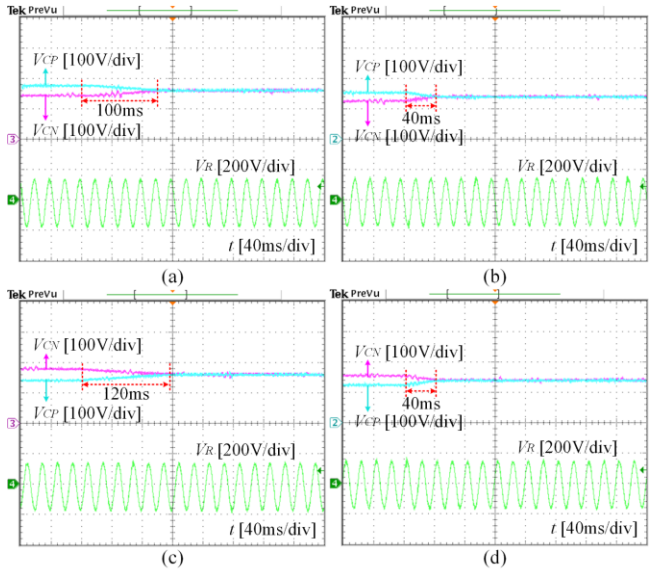

Figure 2.9. Experimental results with the capacitor voltage balancing scheme when (a), (b) $V_{CP} > V_{CN}$, (c), (d) $V_{CP} < V_{CN}$, in which: (a), (c) method [20], (b), (d) proposed method.

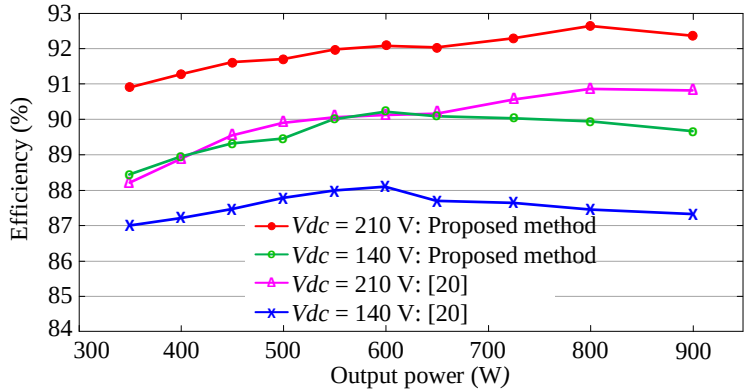

Figure 2.10. Comparison of performance between proposed schemes and schemes [20].

Chapter 3:

PROPOSED SCHEME FOR 3L-qSBT^{2}I CONFIGURATION TO REDUCE COMMON-MODE VOLTAGE

3.1. The proposed CMV reduction scheme for the 3L-qSBT^{2}I configuration.

Table 3.1 CMV of 3L-qSBT^{2}I

Vector		CMV		CMV		CMV
Zero	[OOO]	0	[PPP]	$+V_{PN}/2$	[NNN]	$-V_{PN}/2$
Small vector P	[POO]	$+V_{PN}/6$	[PPO]	$+V_{PN}/3$	[OPO]	$+V_{PN}/6$
	[OPP]	$+V_{PN}/3$	[OOP]	$+V_{PN}/6$	[POP]	$V_{PN}/3$
Small vector N	[ONN]	$-V_{PN}/3$	[OON]	$-V_{PN}/6$	[NON]	$-V_{PN}/3$
	[NOO]	$-V_{PN}/6$	[NNO]	$-V_{PN}/3$	[ONO]	$-V_{PN}/6$
Medium	[PON]	0	[OPN]	0	[NPO]	0
	[NOP]	0	[ONP]	0	[PNO]	0
Large	[PNN]	$-V_{PN}/6$	[PPN]	$+V_{PN}/6$	[NPN]	$-V_{PN}/6$
	[NPP]	$+V_{PN}/6$	[NNP]	$-V_{PN}/6$	[PNP]	$+V_{PN}/6$

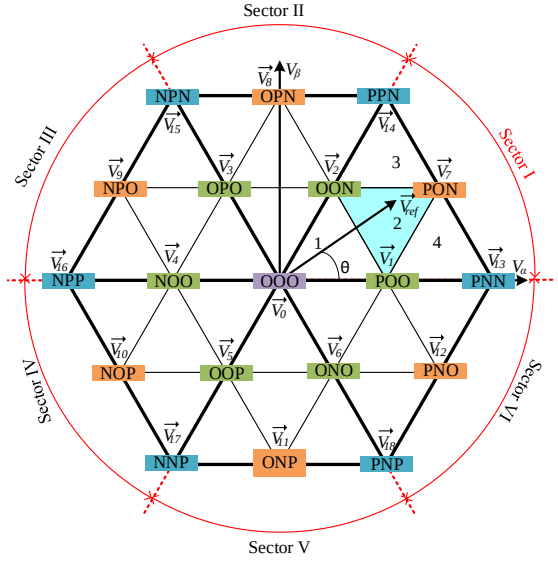

Figure 3.1. Improved space vector diagram.

In the early research introduced in Chapter 2, all 12 small vectors were used to synthesize the reference voltage vector. Therefore, the range of CMV is

from $+V_{PN}/3$ to $-V_{PN}/3$. In this improved SVM scheme, all small vectors produce $\pm V_{PN}/6$ at CMV, zero vector [OOO], medium vector and large vector are used to synthesize the reference vector to decrease the amplitude of CMV.

3.1.1. Calculation of dwell time and switching sequence selection.

In this section, region 2 of sector I is selected to analyze the operation of the proposed scheme. Dwell-times of the component vectors are calculated as shown in Chapter 2. The switching pattern for region 2 of sector I is: [PON]-[POO]-[OON]-[PON] and return, as shown in figure 3.2.

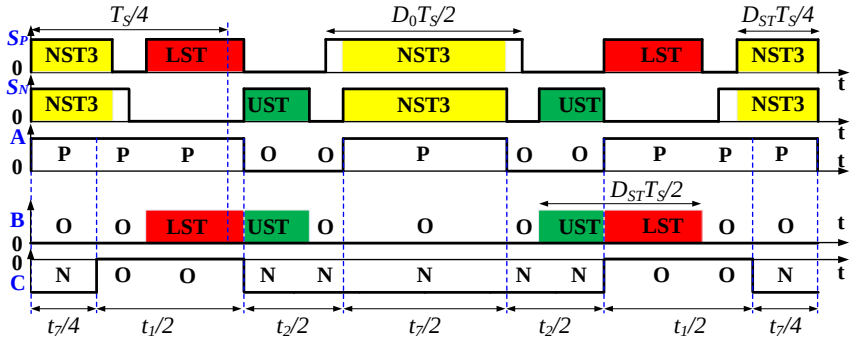

Figure 3.2. Switching sequence for region 2 of sector I.

3.1.2. Neutral voltage balancing.

In order to balance the neutral-point voltage, the on-times of NST 1 and NST 2 are redefined as follows: $(D_1 - D_{ST})T_S/2$ and $(D_2 - D_{ST})T_S/2$, where D_1 and D_2 are defined as the additional duty ratios of switches S_P and S_N. The coefficients D_1 and D_2 can be calculated as follows:

$$\begin{cases} D_1 = D_0 / 2 + k(V_{CP} - V_{CN}) \\ D_2 = D_0 / 2 - k(V_{CP} - V_{CN}) \end{cases} \quad (3.1)$$

3.2. Comparison study

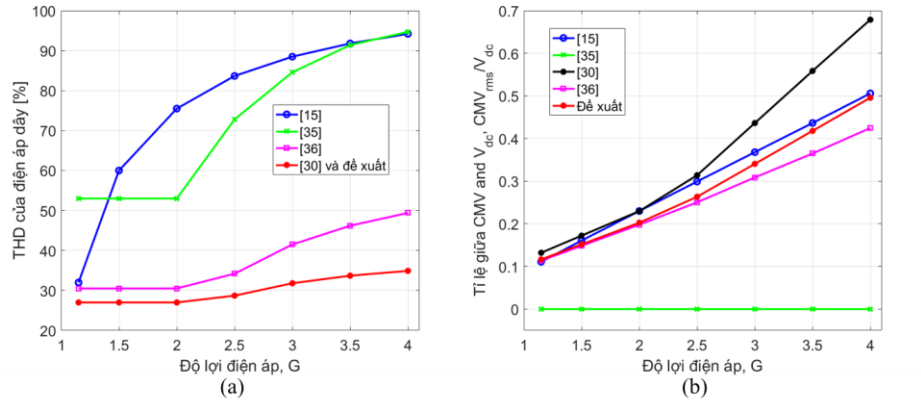

Figure 3.3. Comparison between the proposed method and others.

Overall, the main contribution of this study is to reduce the amplitude of CMV while maintaining the advantages of previous schemes such as high voltage gain and high output voltage quality.

3.3. Experimental results

Table 3.2 Simulation and experimental parameters.

Components		Values
Input voltage	V_{dc}	100 V ÷ 200 V
Output voltage	$V_{o,RMS}$	110 V_{RMS}
Output frequency	f_o	50 Hz
Switching frequency	f_s	5 kHz
Short circuit factor	D_{ST}	0.16
Boost factor	D_0	0.16 ÷ 0.84
Modulation ratio	M	0.92
Inductor	L_B	3 mH/20 A
Capacitor	$C_P = C_N$	2000 µF/400 V
LC filter	L_f và C_f	3 mH và 10 µF
R load	R	40 Ω

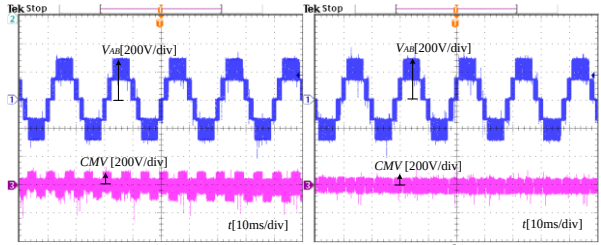

Figure 3.4. Experimental results of the proposed method and [30]. (a) method in [30], (b) proposed method.

Chapter 4:

PROPOSED METHOD FOR TLB-T^{2}I TO SOLVE OCF/SCF AT SWITCHING DEVICES

4.1. Fault tolerant method for TLB-T^{2}I configuration.

In this section, an OCF at a semiconductor device is considered for processing. OCFs are divided into three main categories: 1) The OCF occurs at switch S_P of TLB circuit; 2) The OCF occurs at the switch S_{1A} of 3L-T^{2}I; and 3) The OCF occurs at switches S_{2A} and S_{3A} of 3L-T^{2}I.

4.1.1. Fault-tolerant method for OCF of switch S_P.

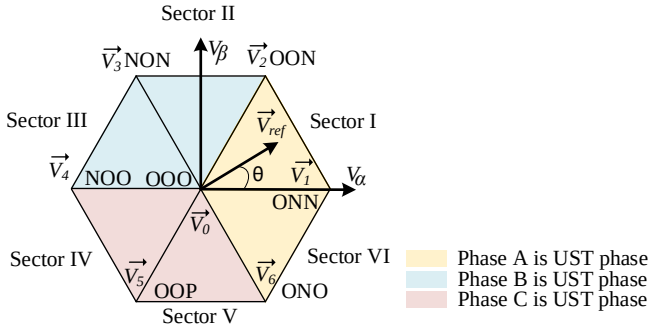

Figure 4.1. SVD to solve OCF of switch S_P.

In order to address the OCF at the switch S_P, the proposed method introduces the inverter to work similarly to the traditional two-stage two-level inverter. In the proposed method, the output of the V_{XO} inverter ($X = A, B, C$) achieves two values of 0-V and -V_{CN} during operation. These two values are represented by the two states [O] and [N] on the SVD. The 0-V value at the output is achieved by simultaneously triggering on two switches S_{2X} and S_{3X}. When two switches S_{3X} and S_{4X} are switched on at the same time, a voltage -V_{CN} is generated at the V_{XO} of the inverter. It can be seen that the switch S_{3X} is always turned on when the proposed method is used. The combination of output voltage states of the

proposed scheme is shown in Figure 4.1. In this scheme, state [NNN] (generated by simultaneously turning on switches S_{4A}, S_{4B}, S_{4C}) is not used.

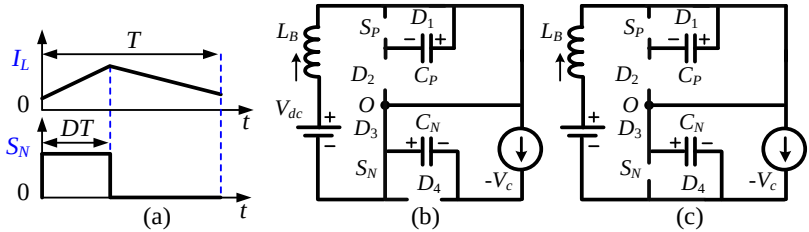

Figure 4.2. (a) Control signal of the switch S_N, (b) mode 1, (c) mode 2.

The boost operation is ensured by controlling the duty cycle of the switch S_N. The control signal of the S_N is shown in Figure 4.2(a).

In this case, the output voltage is defined as follows:

$$V_{x,peak} = \frac{2}{\sqrt{3}} \times M \times \frac{V_{CN}}{2} = \frac{1}{\sqrt{3}} \times M \times \frac{V_{dc}}{1-D} \tag{4.1}$$

The voltage gain of the inverter circuit is calculated as follows:

$$G = \frac{V_{x,peak}}{V_{dc}/2} = \frac{2}{\sqrt{3}} \times \frac{M}{1-D} \tag{4.2}$$

4.1.2. Fault-tolerant method for OCF at switch S_{1A}.

Similar to the OCF at the switch S_P, the OCF at the switch S_{1A} is also handled by controlling the inverter to operate like a two-stage two-level inverter. The operating modes of the TLB-T^{2}I and the control signals of two switches of TLB circuit are presented as shown in Figure 4.3. In this case, the control method of the switch SP is always turning on and the control-signals of the switches S_{1A}, S_{1B}, and S_{1C} of the inverter side are always turning off. This causes the capacitor C_P to be isolated from the power circuit. Diode D_1 is reverse-biased, while diode D_2 is forward-biased. The two main operating modes of the inverter circuit are determined by the switching state of the switch S_N.

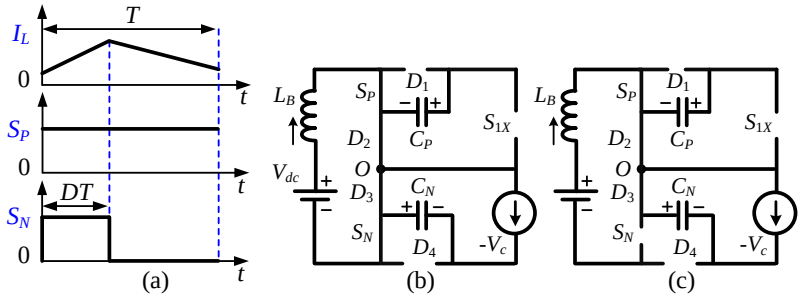

Figure 4.3. (a) Control signal of the switches S_P, S_N, (b) mode 1, (c) mode 2.

The proposed scheme controls the 3L-T^{2}I circuit, which acts like a traditional two-level inverter, by turning off the control signals of three switches (S_{1A}, S_{1B}, and S_{1C}). The combination of output voltage states of the proposed scheme is similar to the OCF at S_P. However, the vector [NNN] is still used in this case.

4.1.3. Fault-tolerant method for OCFs at switches S_{2A} and S_{3A}.

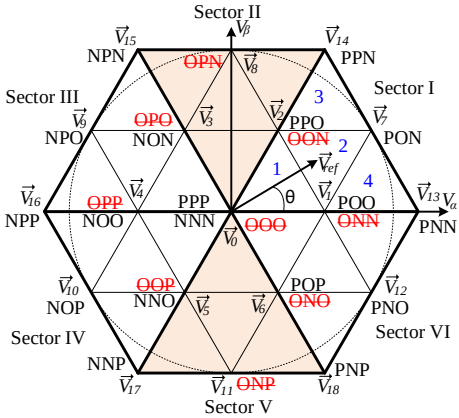

Figure 4.4. SVD of FT method for OCFs at switches S_{2A} and S_{3A}.

To solve this OCF, an improved space vector scheme was used. The SVD of this OCF is shown in Figure 4.4. It can be seen that when the OCF occurs at S_{2A} and S_{3A}, zero vector [OOO], small vectors [ONN], [OON], [OPO], [OPP], [ONO], and two medium vectors [OPN] and [ONP] cannot be achieved at the output of the inverter. Unlike medium vectors, small vectors and zero vectors

always have redundant vectors. Therefore, the operation of the inverter in sectors I, III, IV, and VI can be guaranteed to be similar to that in the normal operation with the help of redundant vectors. Since the medium vectors [OPN] and [ONP] have no redundant vectors, the operation of the inverter in sectors II and V cannot be maintained as that in the normal operation. In this case, the proposed scheme controls the inverter to act as a 2-level inverter by using zero and large vectors to modulate the output vector.

4.2. Comparison between the proposed scheme and the traditional schemes

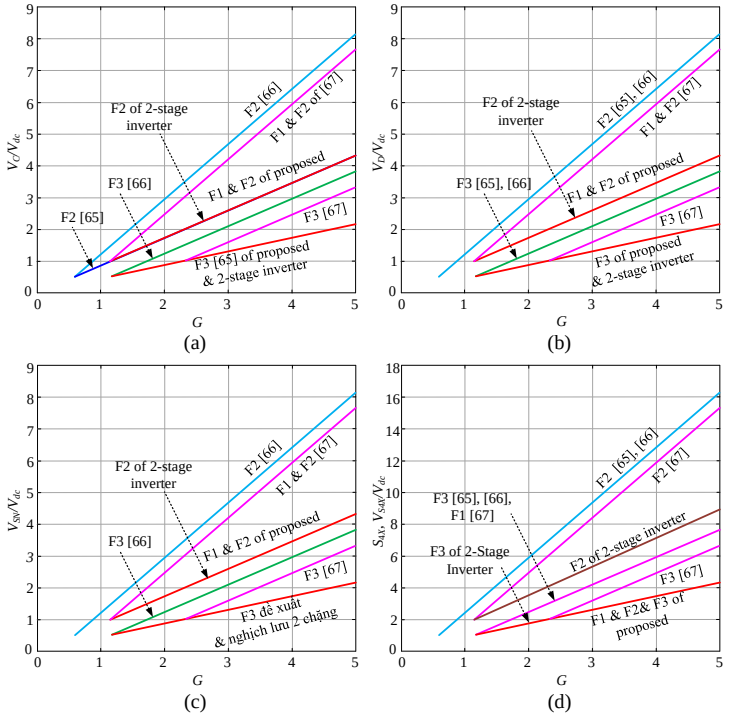

Figure 4.5. Comparison between the proposed scheme and the traditional scheme: (a) G and voltage across capacitor, (b) G and voltage across the diode, (c) G and voltage across the switch S_P/S_N, (d) G and voltage across the switch S_{4X} on the inverter side.

The investigations of component voltage rating for different fault-tolerant schemes are presented in Figure 4.5. In these studies, the proposed method and traditional 2-stage inverter configuration show superiority in generating smallest component voltage rating because they have a higher modulation index than the other studies. Especially for the open-circuit fault occurring at S_{1A}, the proposed method can reduce the voltage rating on the switches S_{1X}/S_{4X} by ½ compared to the traditional 2-stage configuration, shown in Figure 4.5(d).

4.3. Experiment with the proposed scheme.

Table 4.1 Experimental parameters

Parameters / Components		value
Input voltage	V_{dc}	200 V
Output voltage	$V_{x,RMS}$	110 V_{RMS}
Output frequency	f_0	50 Hz
Switching frequency	f_s	10 kHz
Booster inductor	L_B	3 mH/20 A
Capacitor	C_P and C_N	1 mF/400 V
Filter circuit	L_f and C_f	3 mH and 10 µF
Load	R_X	40Ω

Table 4.2. Capacitor voltages and THD output line-to-line voltage

	Normal	F1	F2	F3
V_{CP}	200 V	200 V	0 V	200 V
V_{CN}	200 V	400 V	400 V	200 V
THD_{VAB}	49.4 %	96.3 %	99.8 %	66.7 %

Three FT methods at the switches S_P (F1), S_{1A} (F2), and bidirectional semiconductor switches S_{2A} and S_{3A} (F3) are demonstrated in this section. Note that the fault diagnosis method will not be mentioned because these methods have been thoroughly addressed in previous studies. The operation parameters of the inverter circuit are mentioned in Table 4.1. Capacitor voltage and THD value of V_{AB} are listed in Table 4.2.

4.3.1. Results for the FT method at the switch S_P

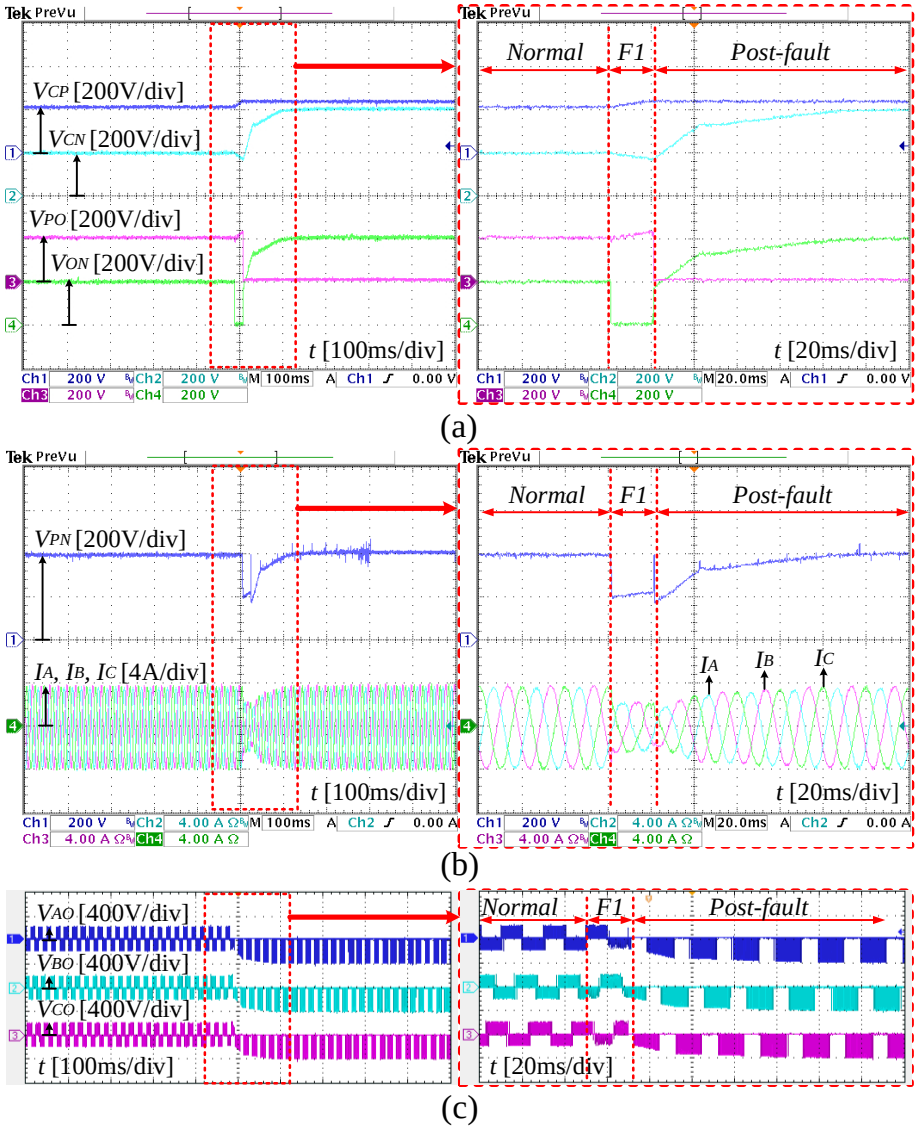

Figure 4.6. Experimental results of the FT scheme for OCF at S_P.

4.3.2. Results for FT method at the switch S_{1A}

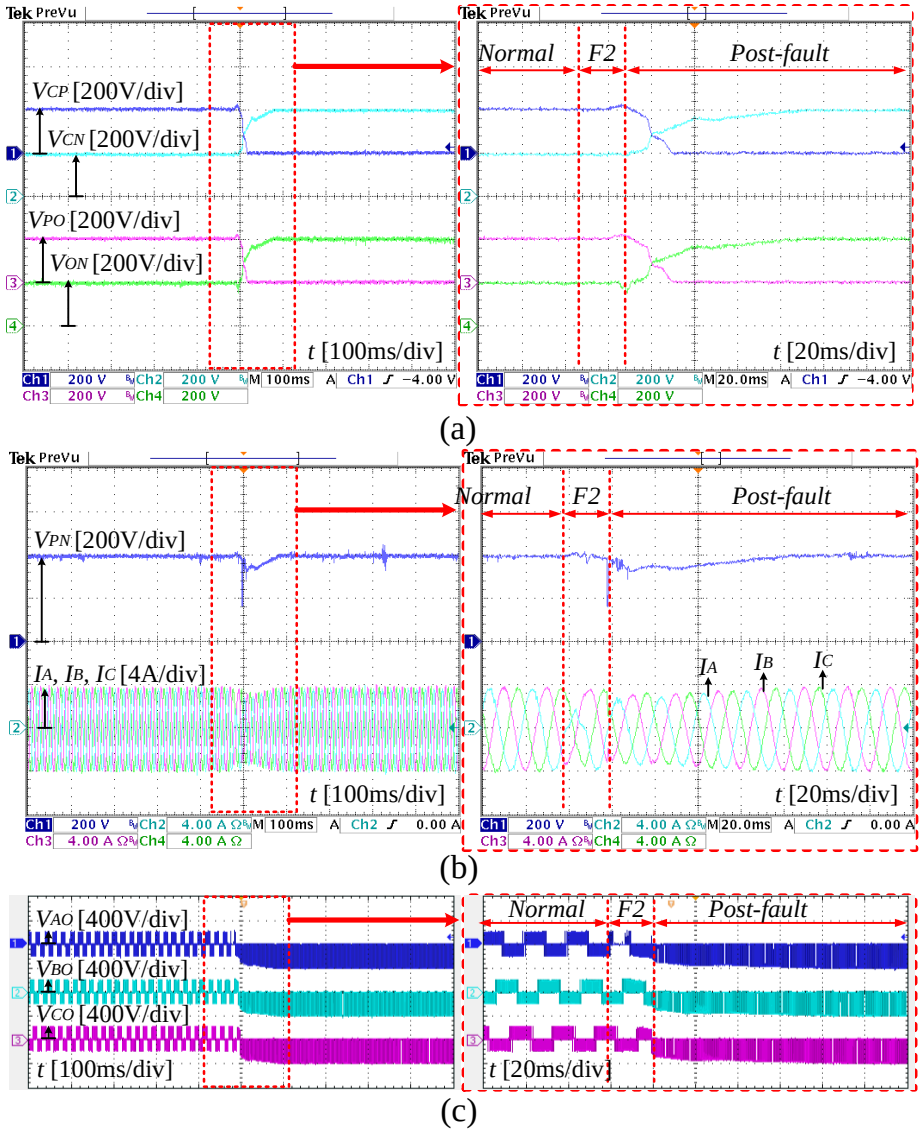

Figure 4.7. Experimental results of the FT scheme for OCF at S_{1A}.

4.3.3. Results for the FT method at the switches S_{2A} and S_{3A}

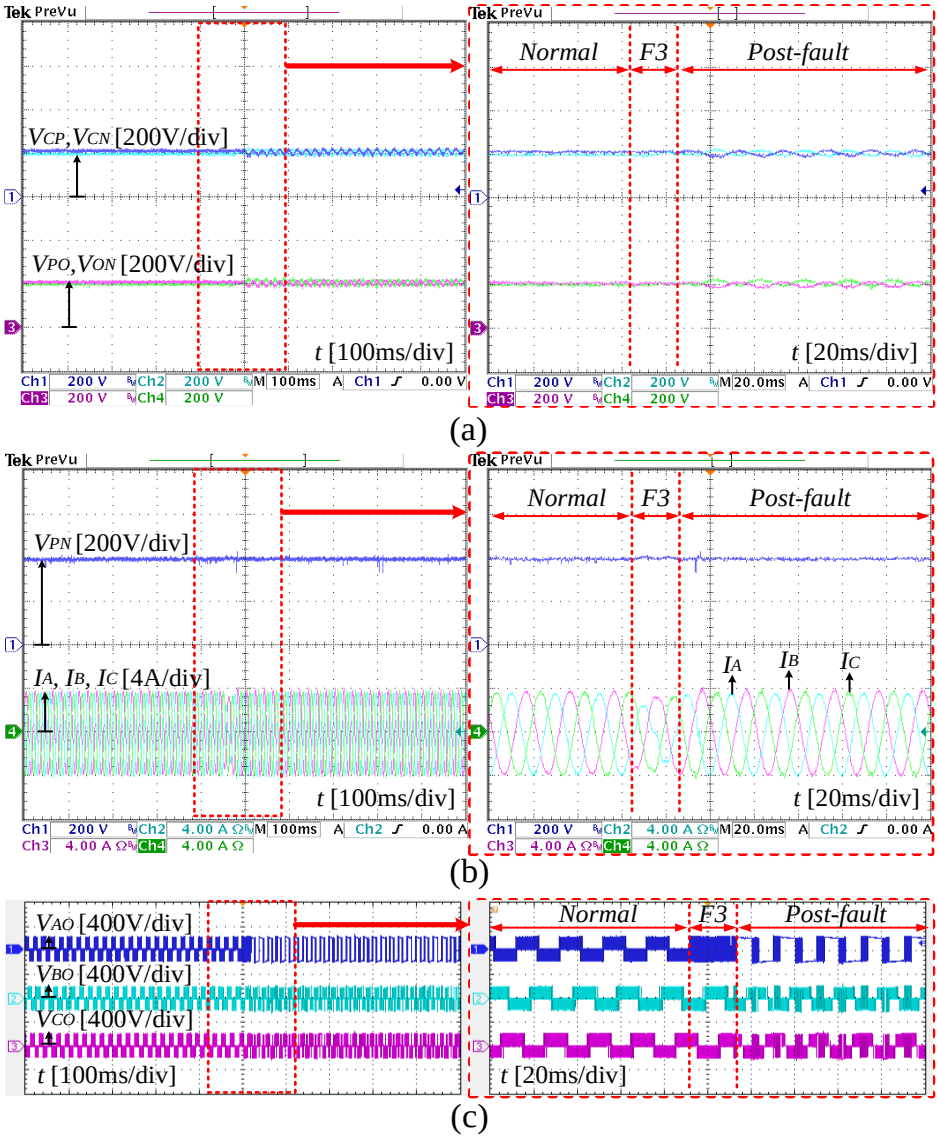

Figure 4.8. Experimental results of the FT scheme for OCF at S_{2A} and S_{3A}.

4.3.4. Efficiency of the inverter circuit

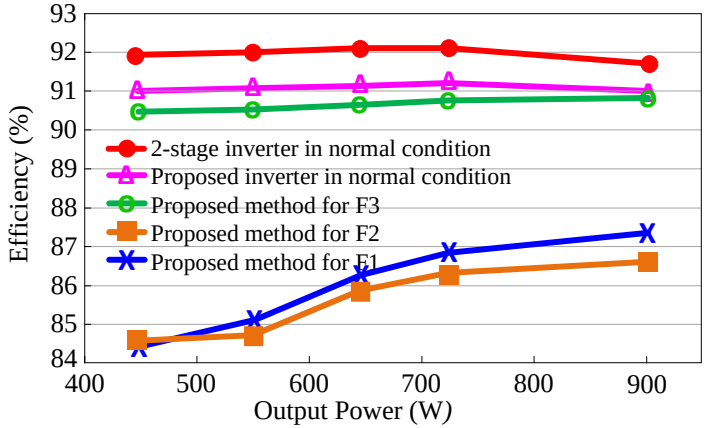

Figure 4.11. Efficiency of the inverter circuit.

Chapter 5:

CONCLUSION AND DEVELOPMENT DIRECTION

5.1. Conclusion

From the obtained results of the thesis, some conclusions are drawn as follows:

- The thesis has presented the urgency of using inverters for the development of current and future energy trends.
- The thesis has presented the advantages and disadvantages of single-stage inverters and control schemes under normal conditions, as well as the faults that occurred in power switches.
- The space vector modulation scheme is presented specifically in the thesis to enhance voltage gain and balance capacitor voltages (Chapter 2).
- The improved space vector modulation scheme is specifically presented in the thesis to reduce the effective amplitude as well as the peak-peak amplitude of the common-mode voltage (Chapter 3).
- The space vector modulation scheme for open-circuit and short-circuit faults occurring at power switches and capacitors is also presented in detail in the thesis (Chapter 4).

With the presented schemes, the inverter circuit can improve efficiency, voltage stress of components. These advantages have been verified through comparison, simulation, and experiment.

5.2. Limitations and development direction of the thesis

Besides the above advantages, the thesis still has some limitations, such as:

- The experimental prototype was built to verify the proposed scheme; therefore, it has not been optimally designed. For safety reasons, the experimental power is only about 1 kW. The enhancement of experimental

capacity is not considered in this thesis.

- Due to research funding constraints, modern semiconductor devices such as silicon carbide (SiC) or gallium nitride (GaN) have not been used. Therefore, the efficiency of the whole system is generally still low compared to commercial products on the market. In addition, the scheme is tested on a resistive load, which is one of the limitations of the thesis.

From the limitations listed above, the future development direction of the thesis can be listed as follows:

- PCB circuits with optimally selected components for commercial products will be developed in the future.

- The proposed schemes will be considered and verified with grid-tied solar applications in the future.